



FIG. 1

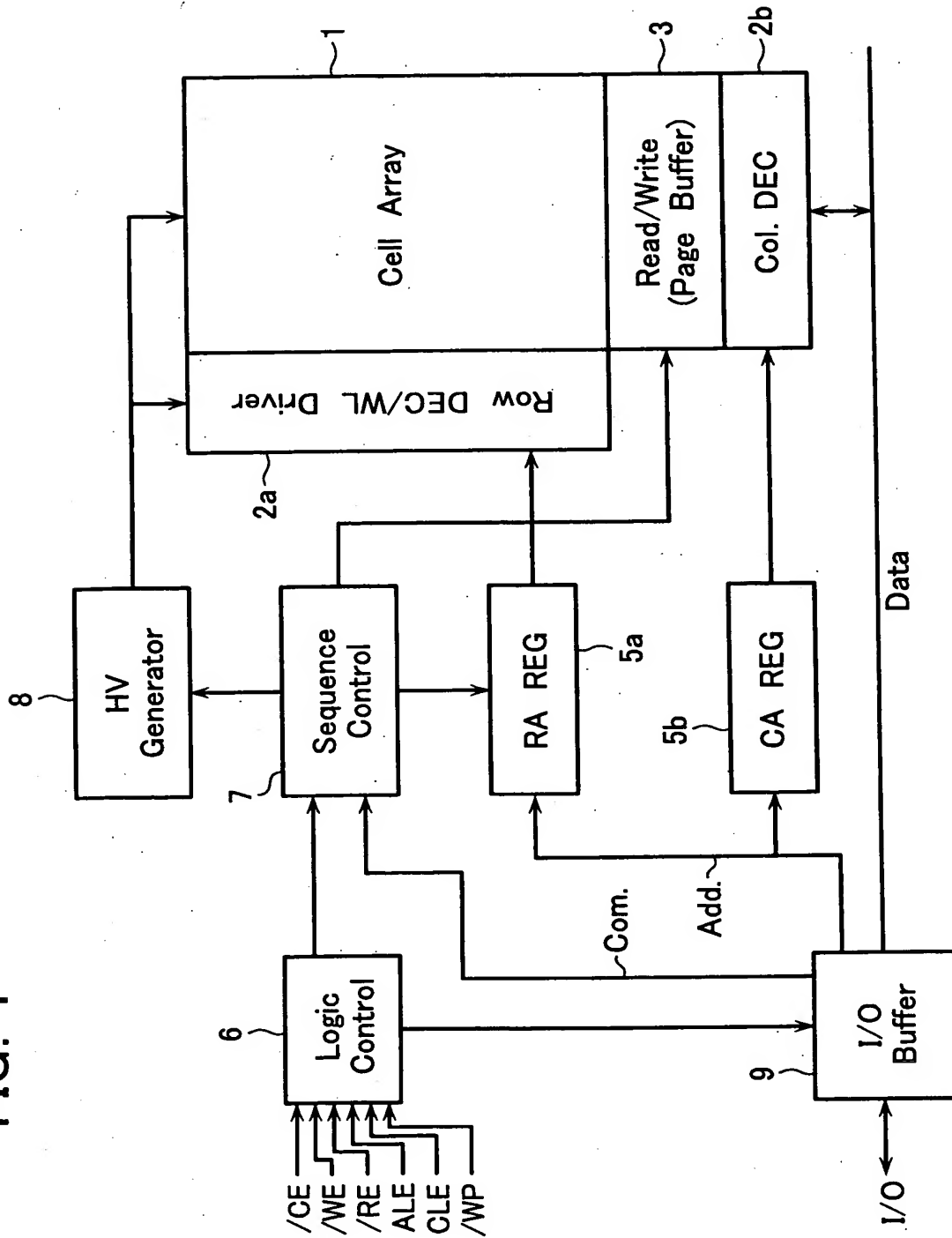




FIG. 2

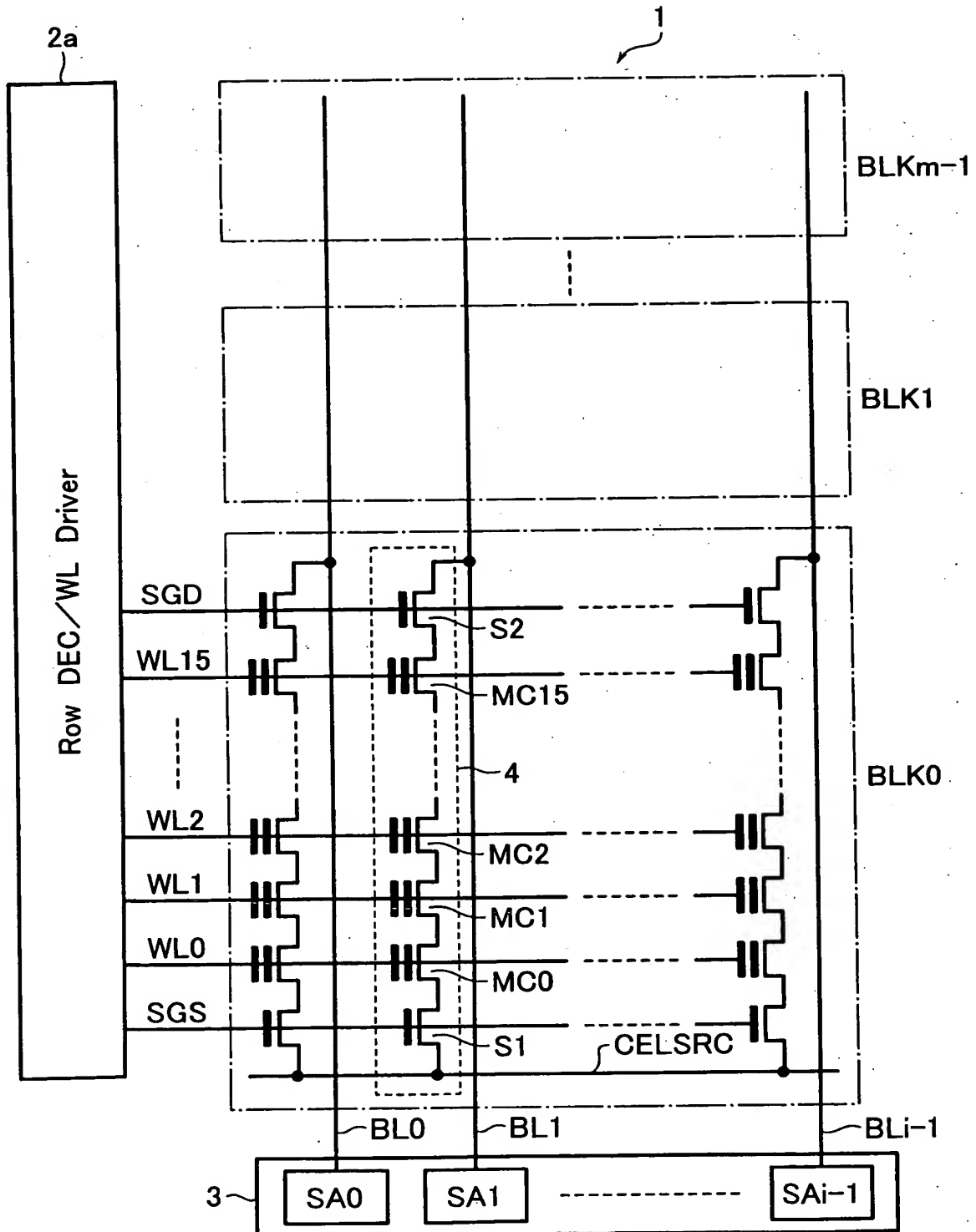
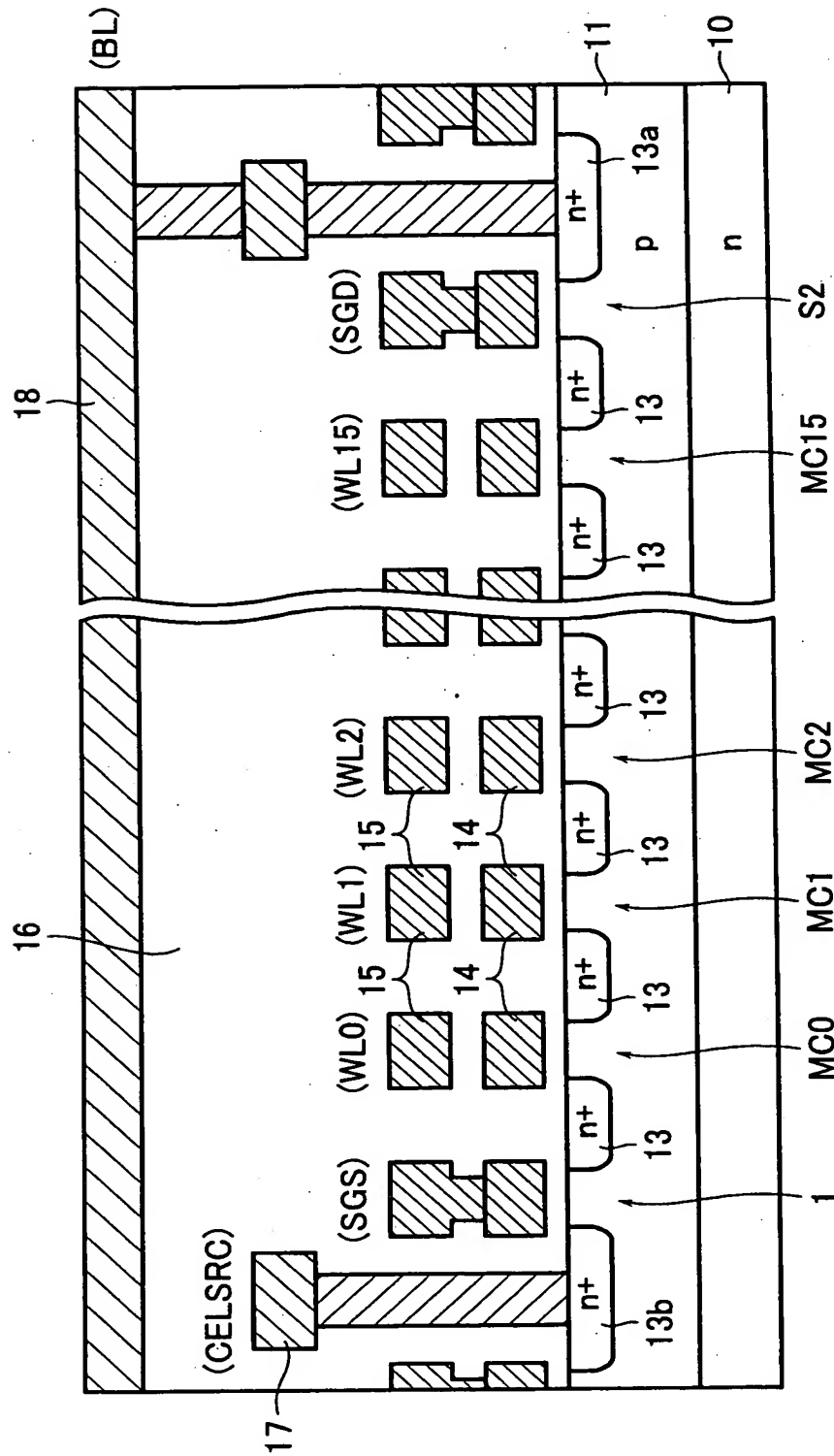




FIG. 3



The diagram illustrates a semiconductor device 4, which is a pixel array. It features a series of word lines (WL0, WL1, WL2, ..., WL15) and a source line (SGS). A gate driver circuit (SGD) is connected to the word lines. The pixel array consists of a series of transistors (S1, S2, ..., S15) connected to the source line. Each transistor S_i is connected to a word line WL_i. The output of the pixel array is connected to a sense amplifier (SA) circuit. The sense amplifier circuit includes a series of transistors (N1, N2, ..., N15) and capacitors (C1, C2, ..., C15). The sense amplifier circuit is connected to a sense line (SEN) and a sense amplifier output (SAO). The sense amplifier circuit also includes a sense amplifier input (SAI) and a sense amplifier output (SAO). The sense amplifier circuit is connected to a sense line (SEN) and a sense amplifier output (SAO). The sense amplifier circuit also includes a sense amplifier input (SAI) and a sense amplifier output (SAO).



FIG. 5

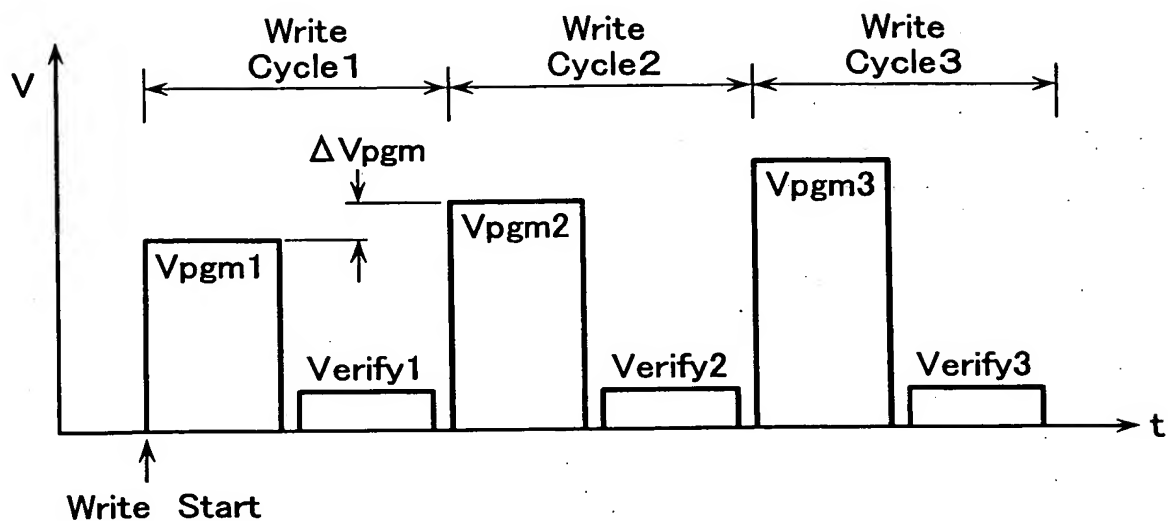


FIG. 6

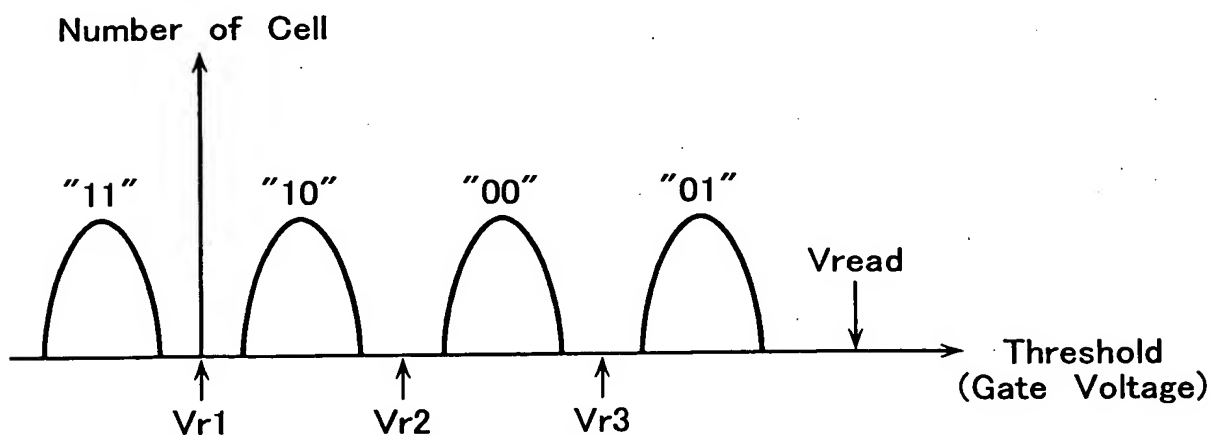




FIG. 7

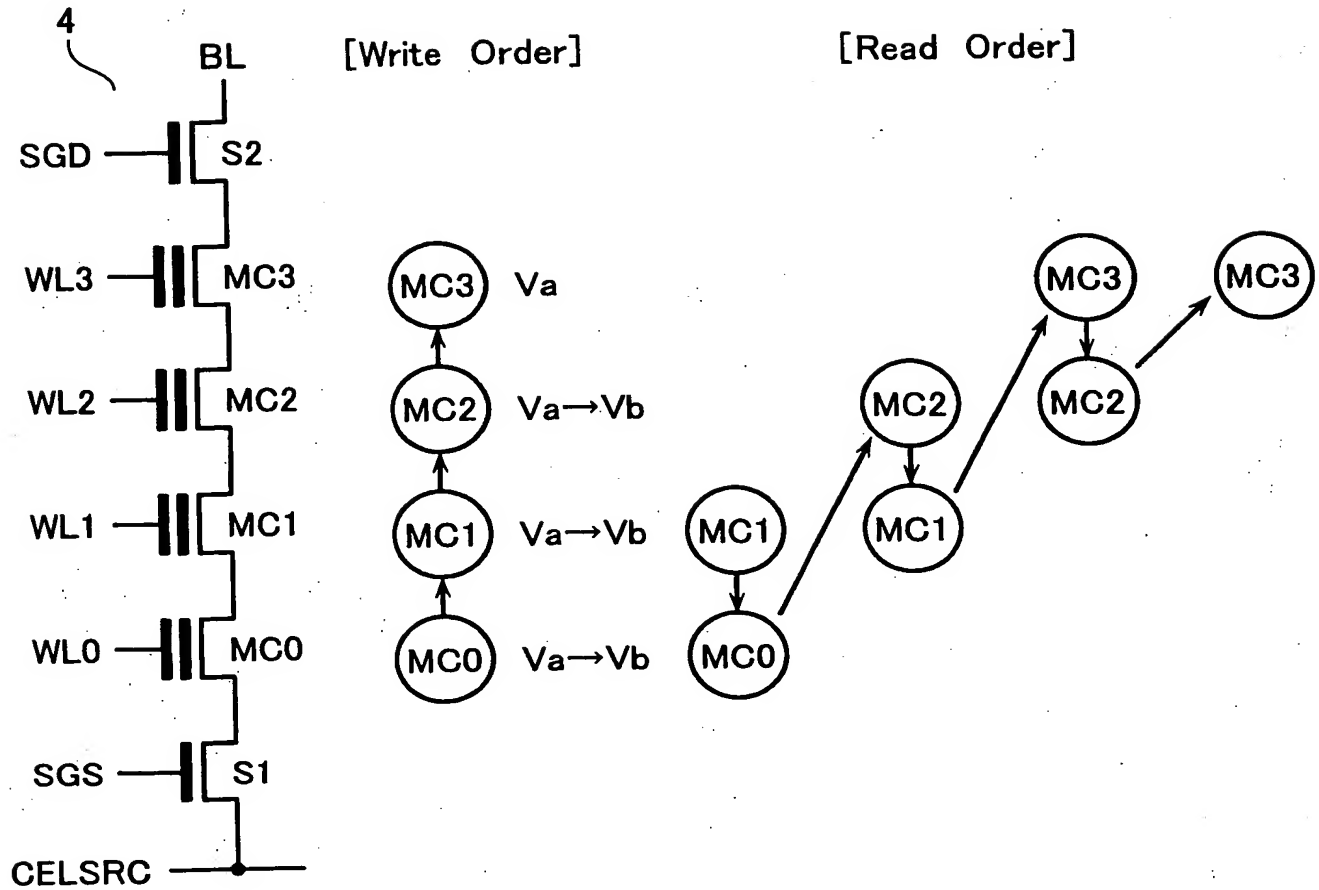




FIG. 8

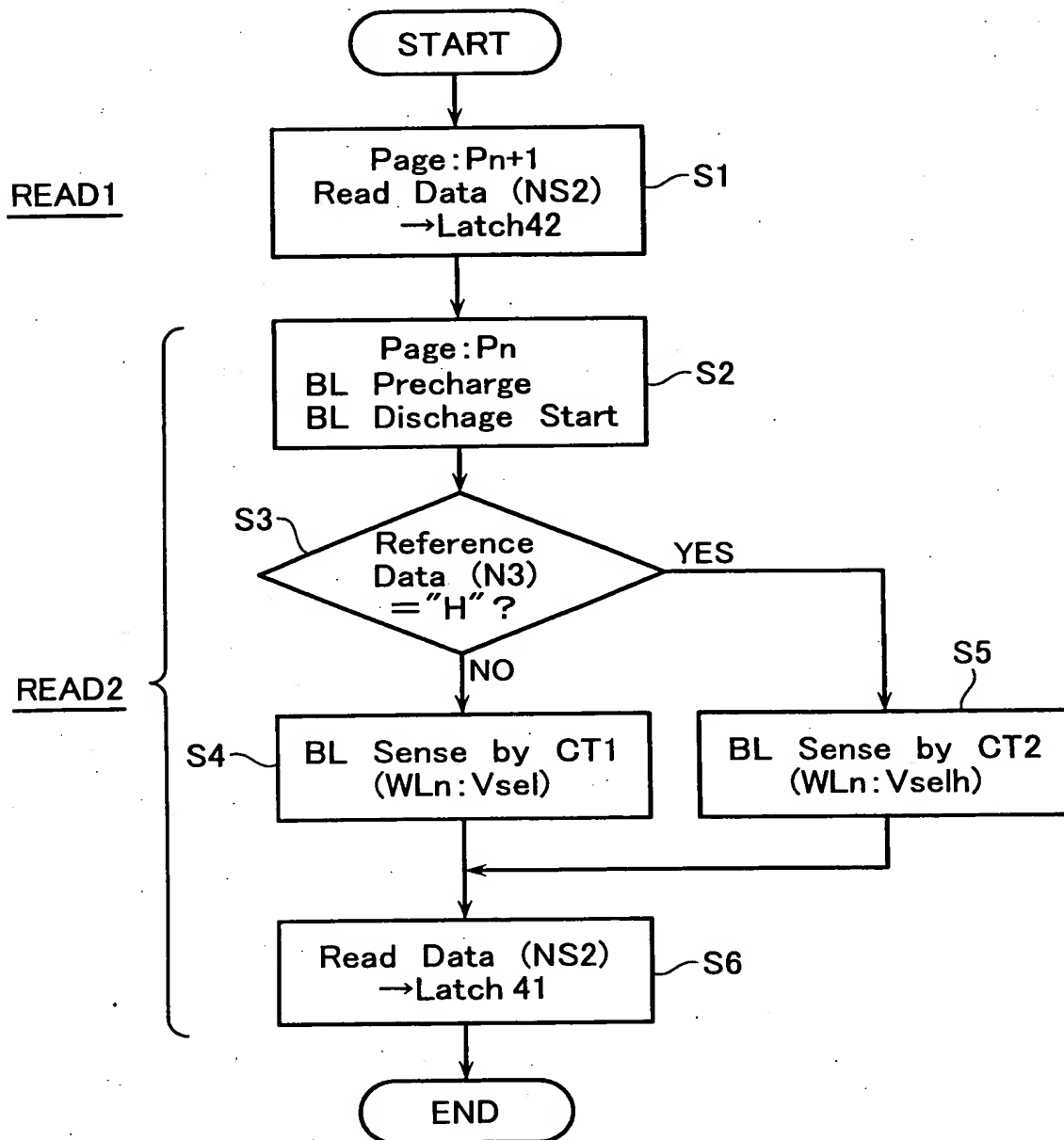


FIG. 9A

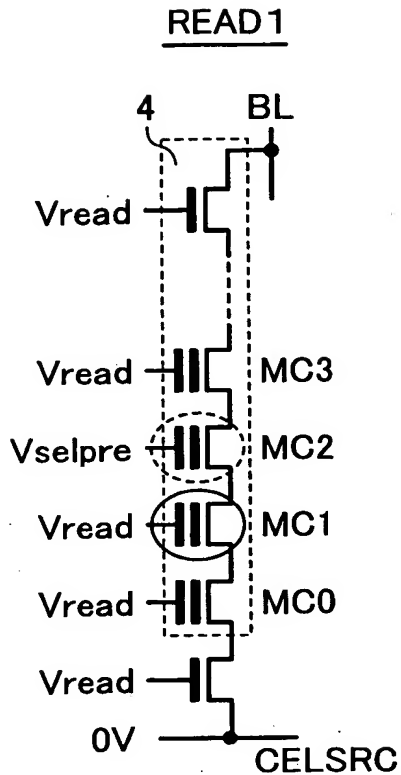


FIG. 9B

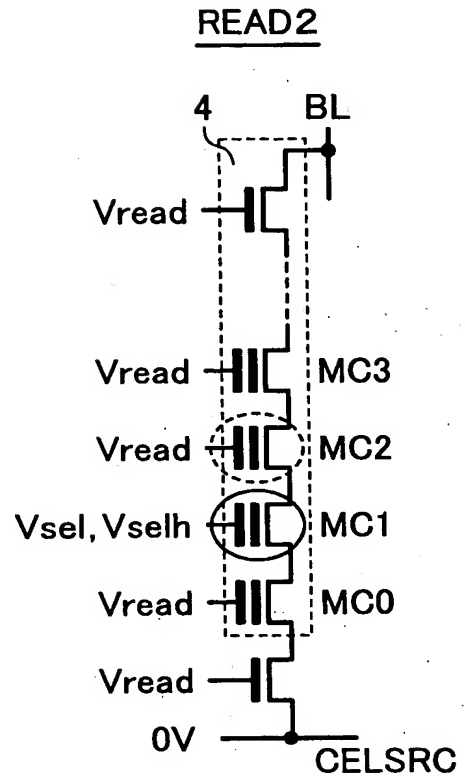


FIG. 10

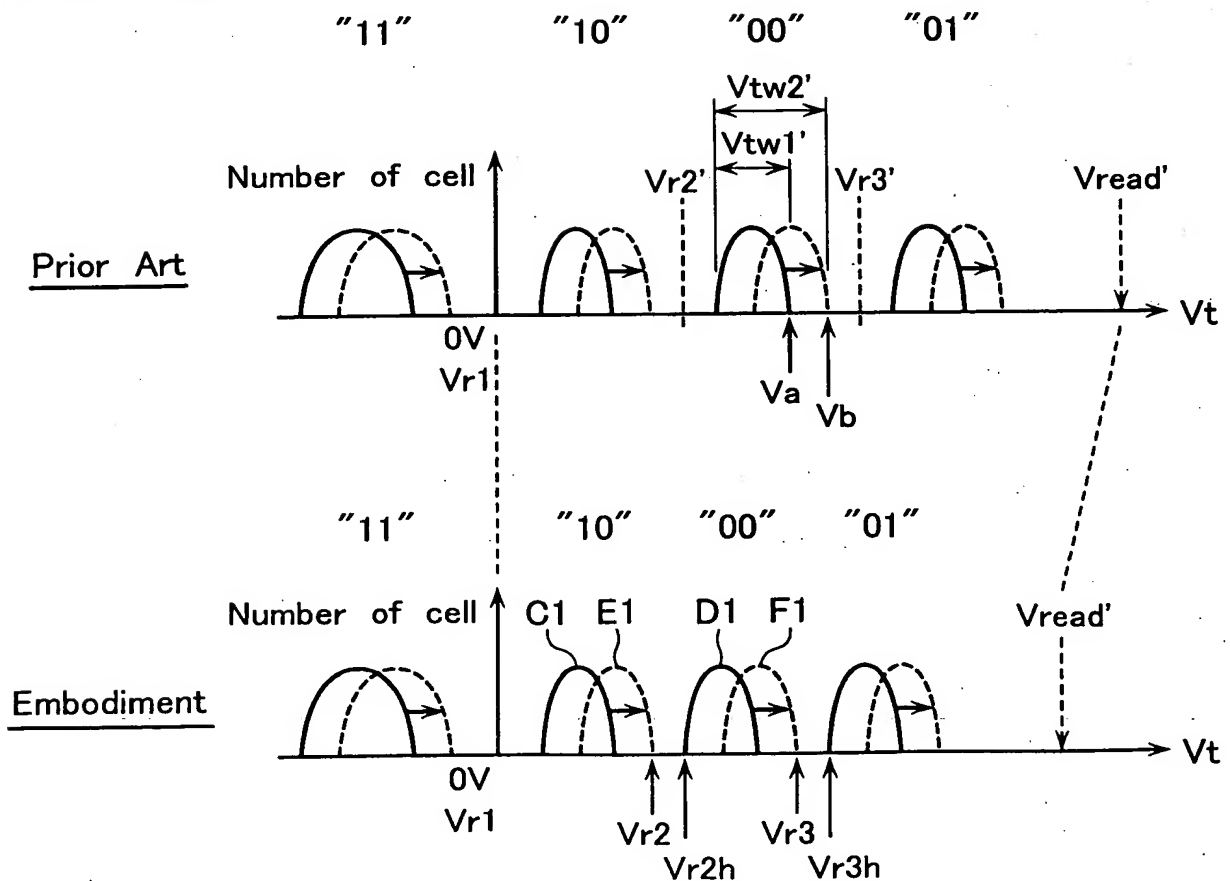




FIG. 11

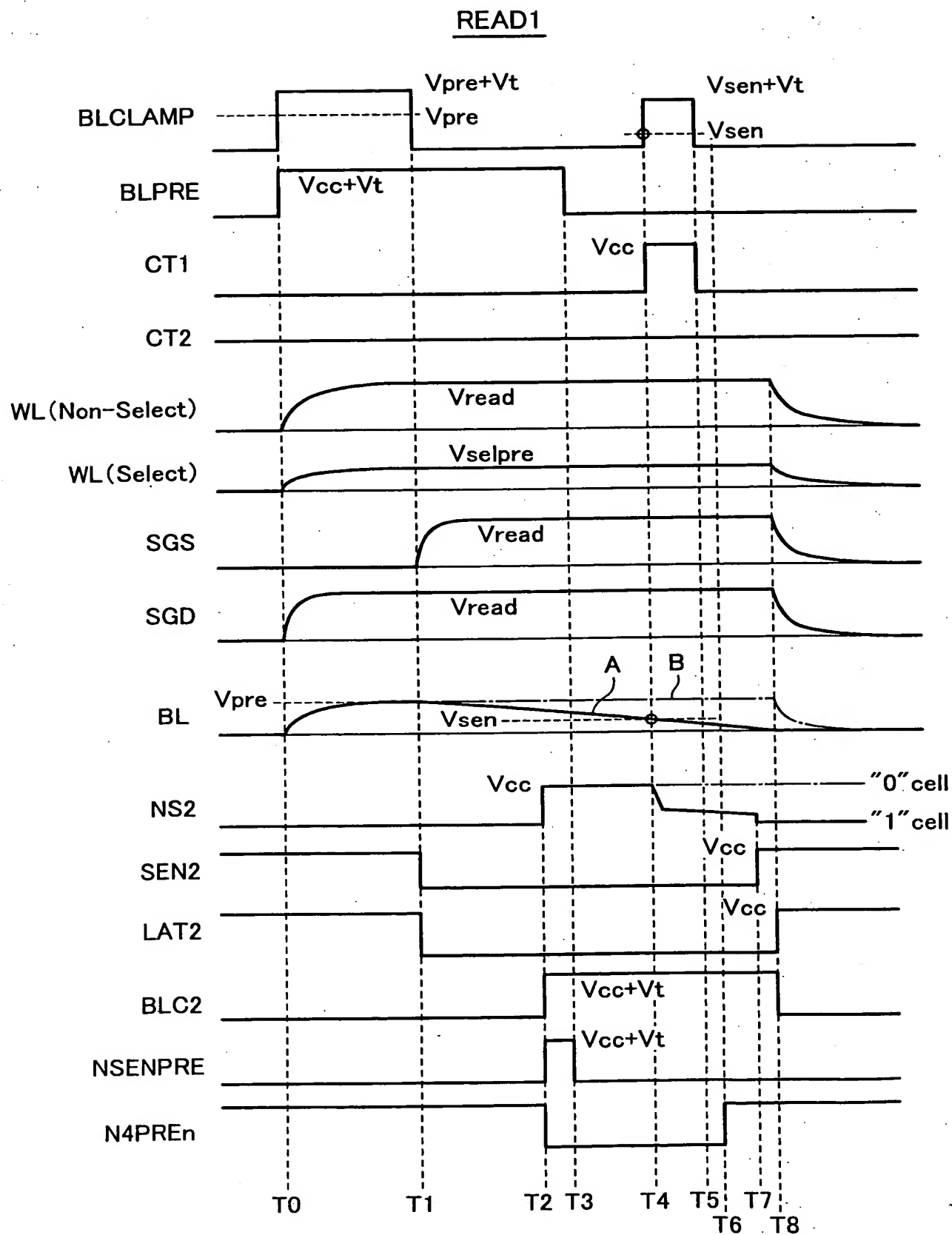




FIG. 12

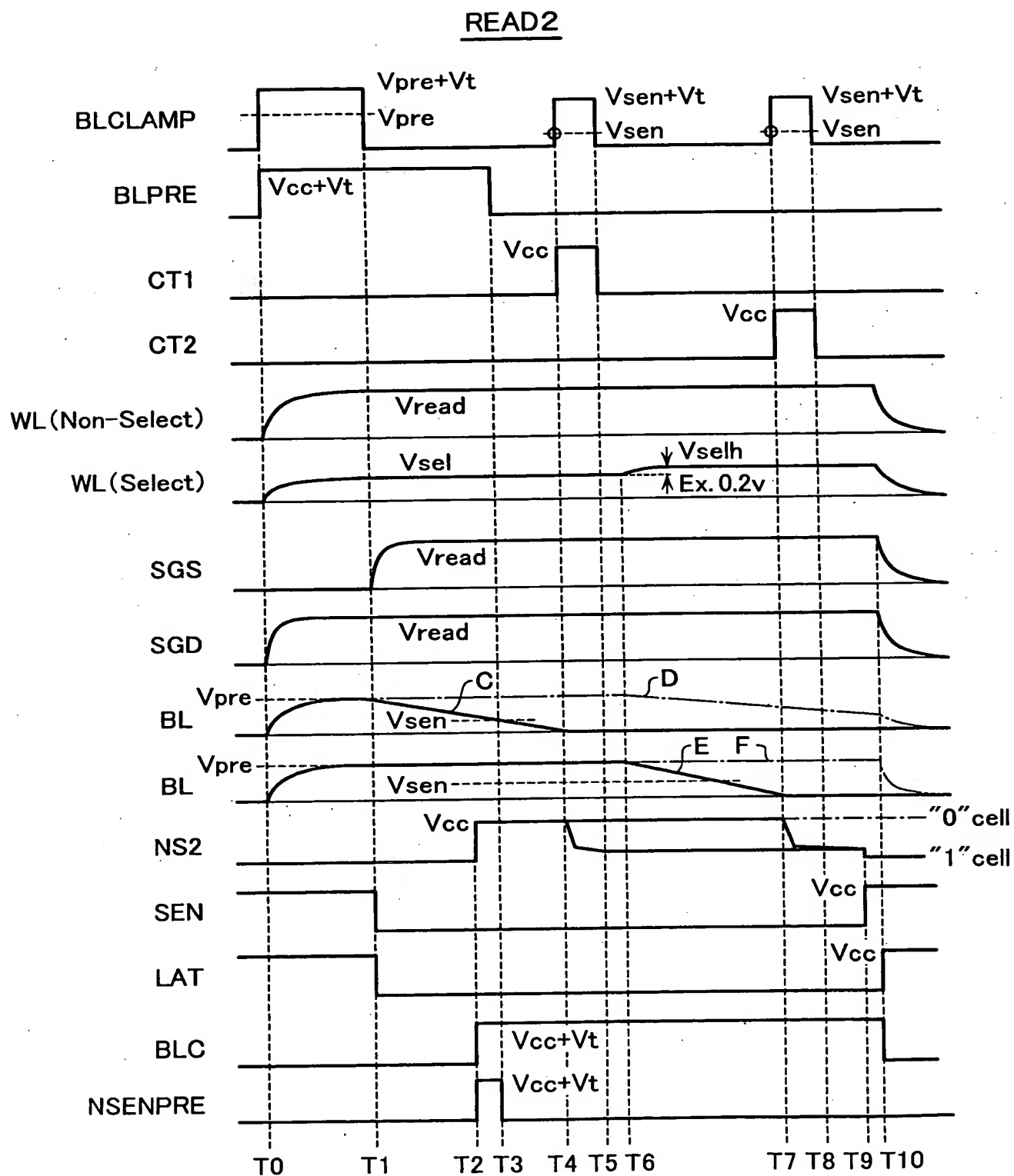




FIG. 13

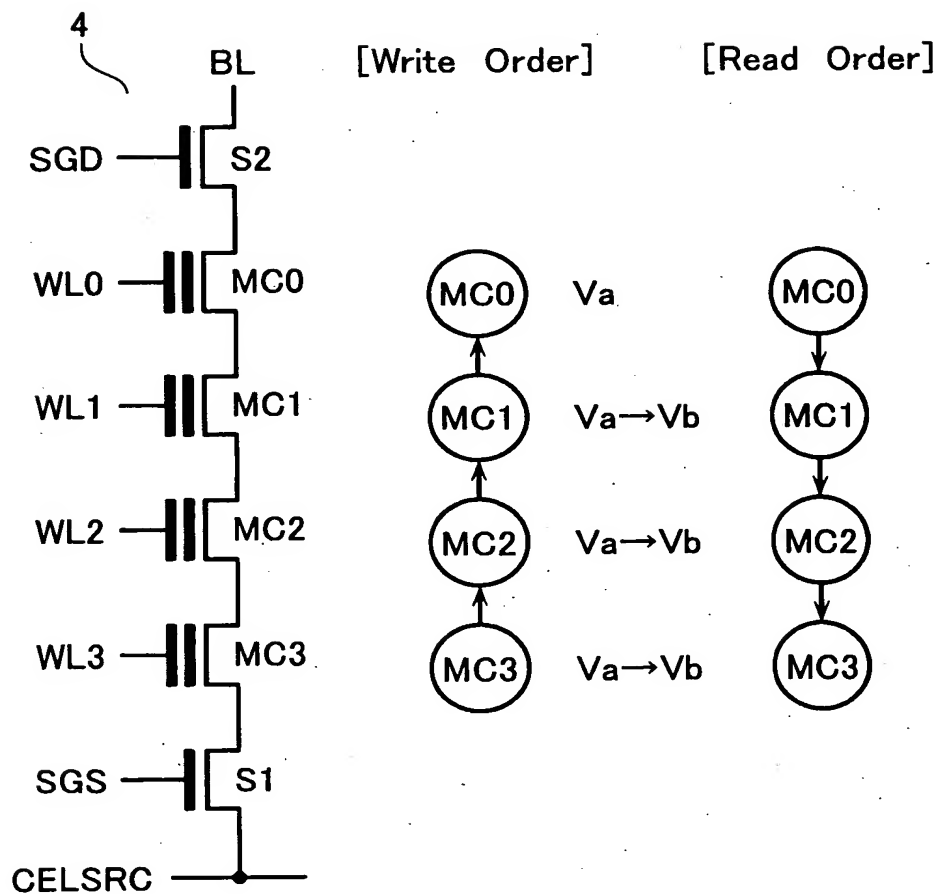




FIG. 14

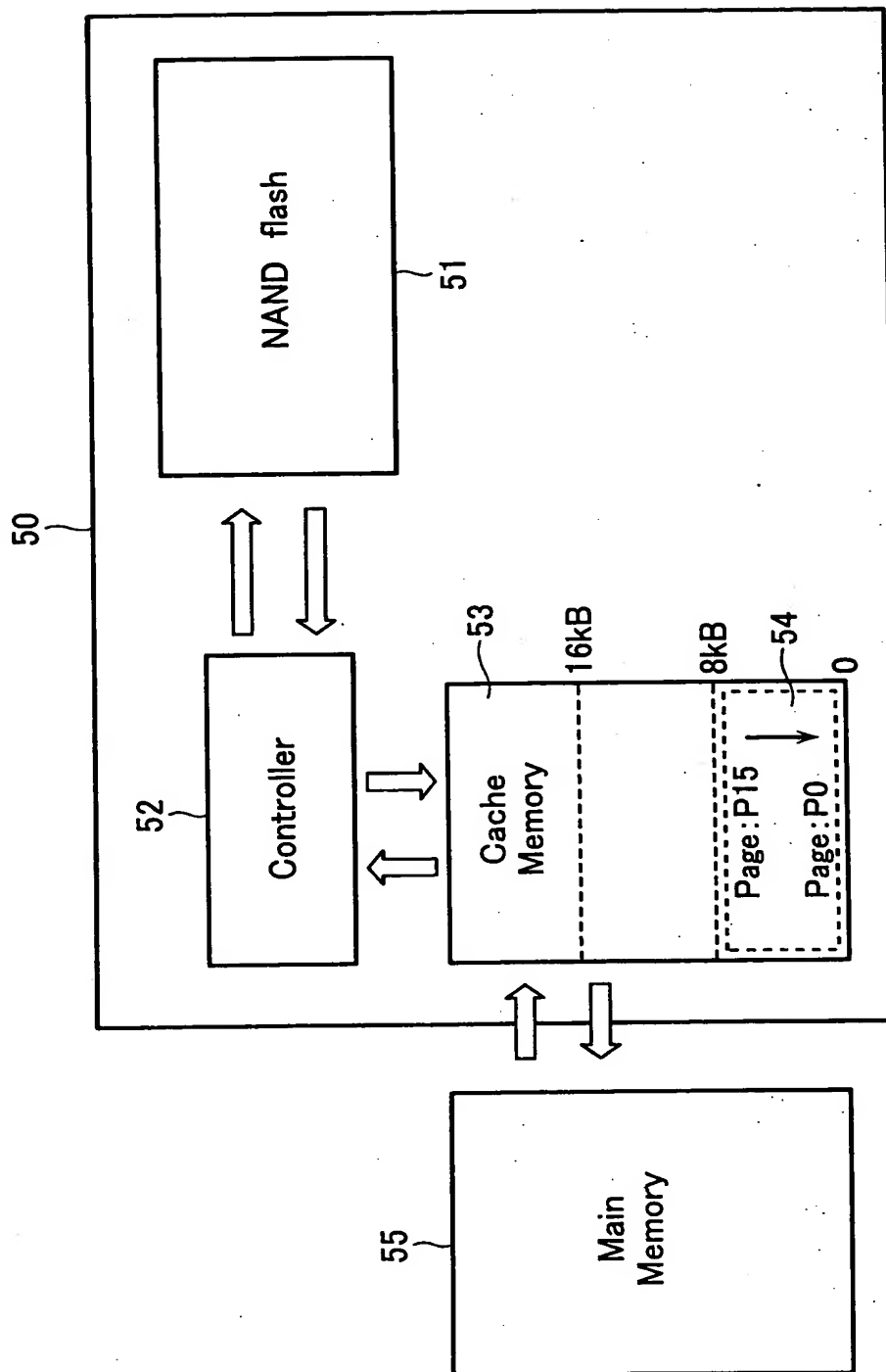




FIG. 15

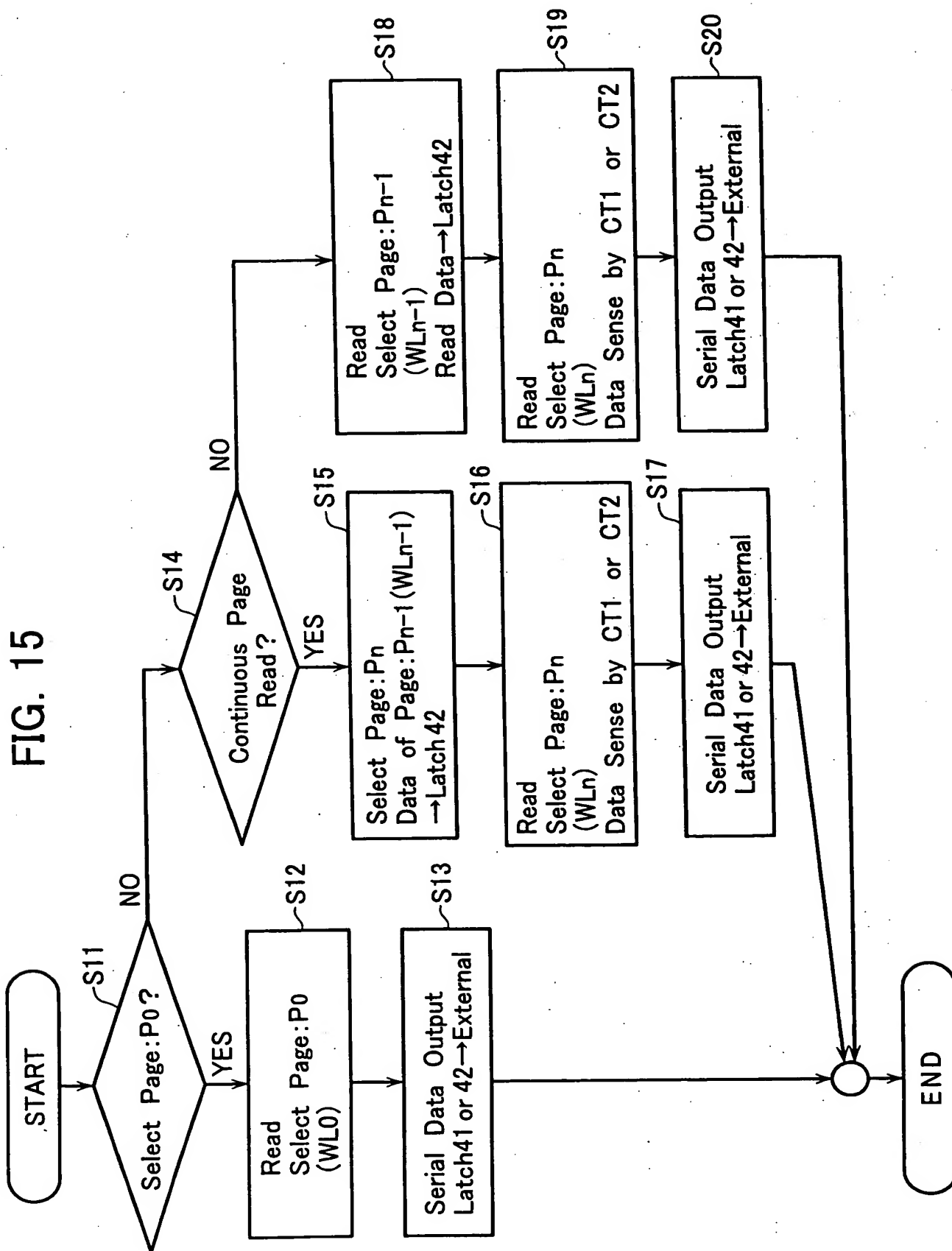




FIG. 16

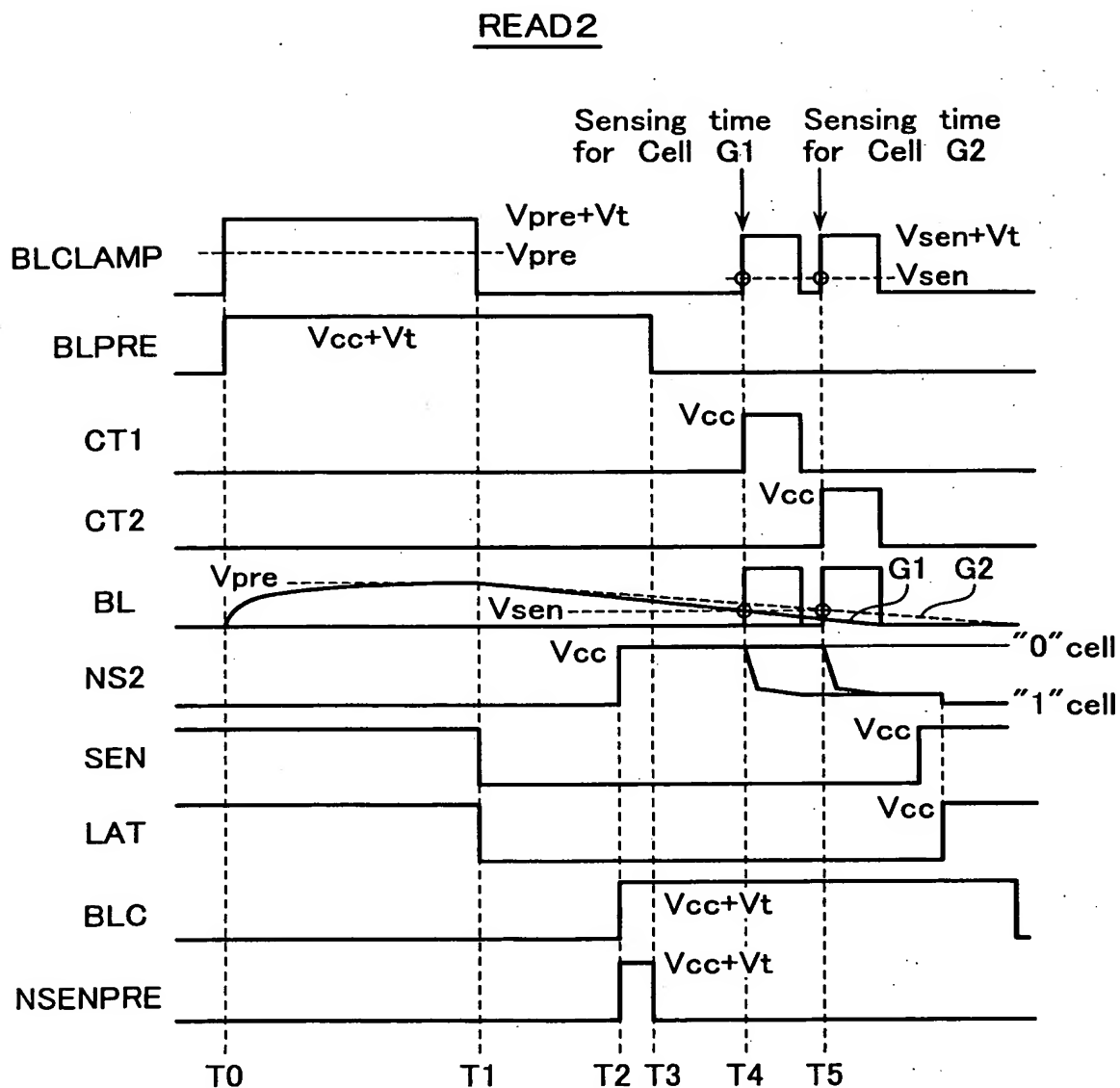




FIG. 17

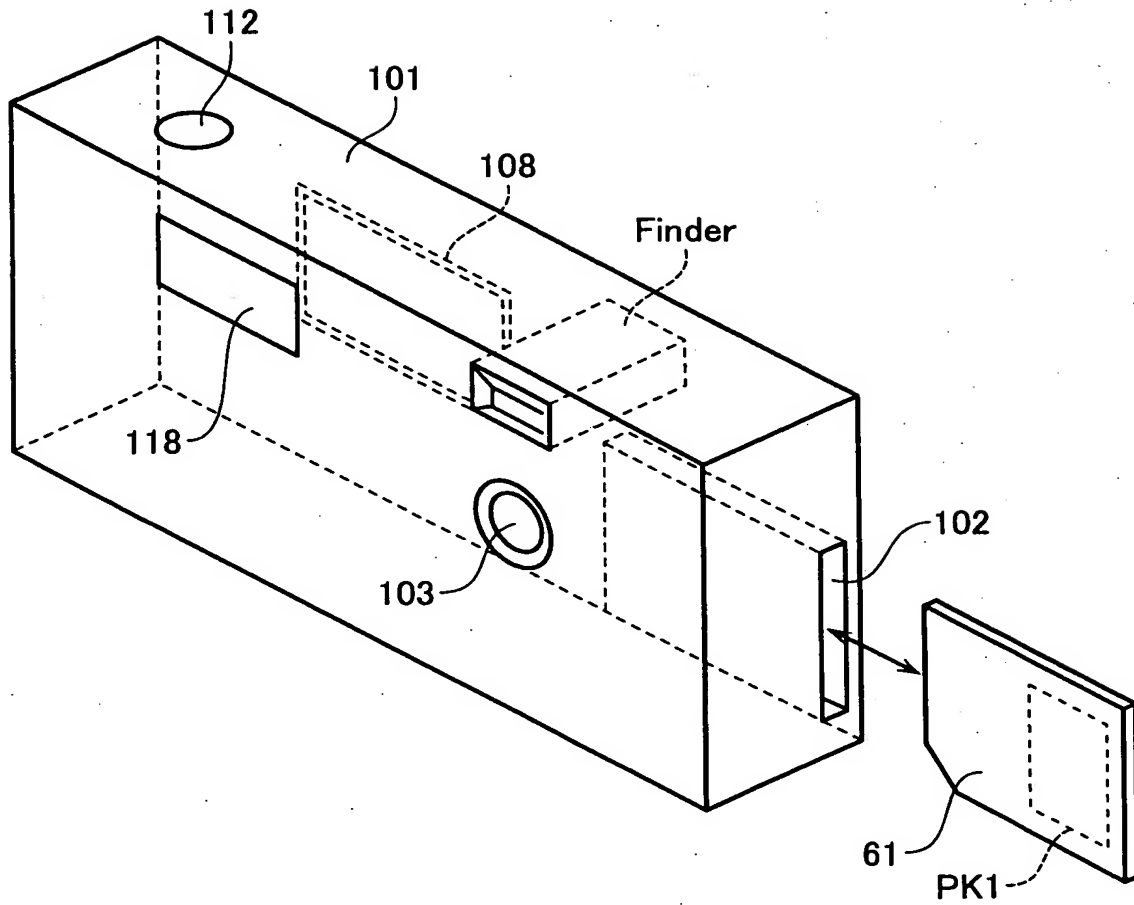




FIG. 18

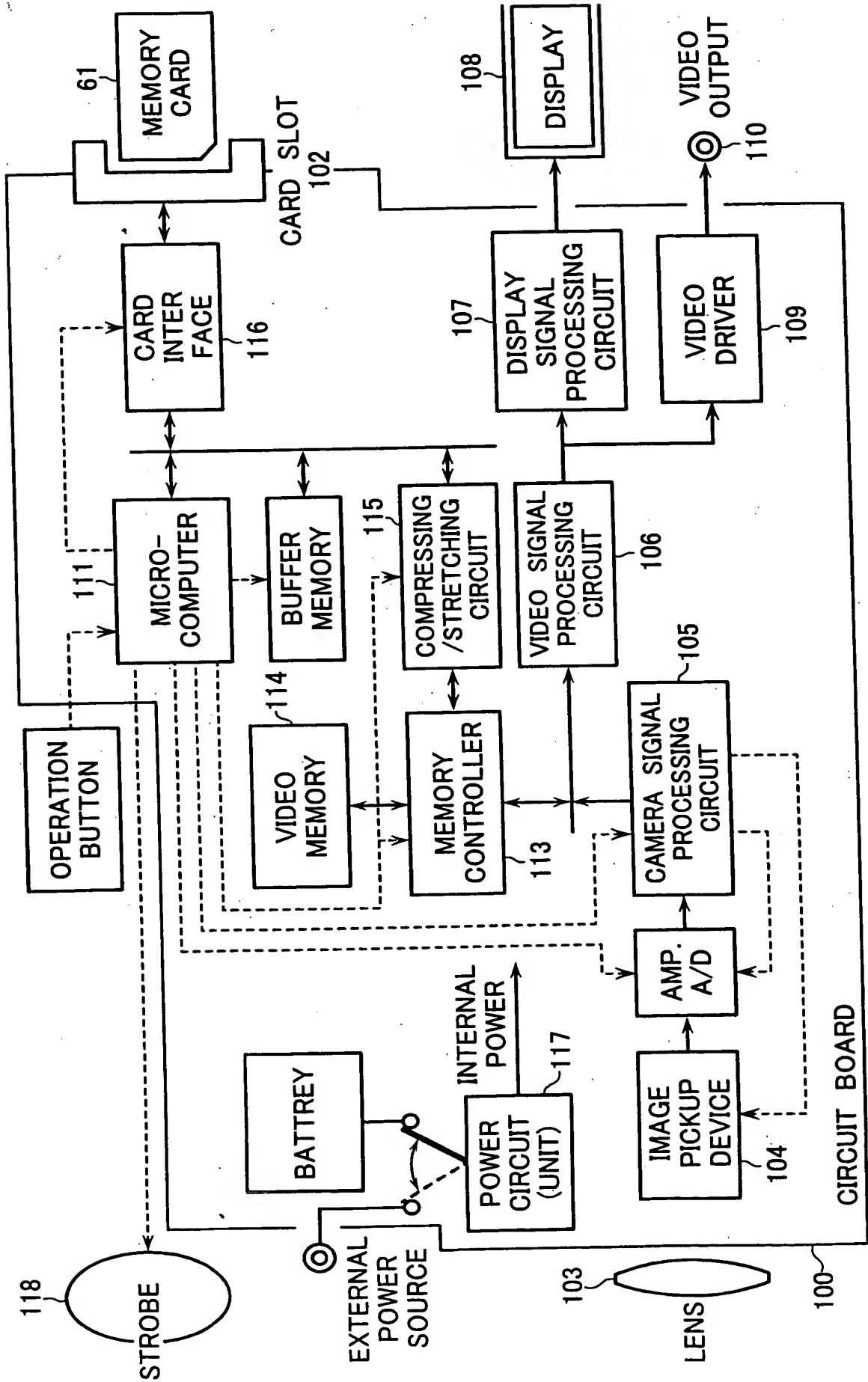




FIG. 19A

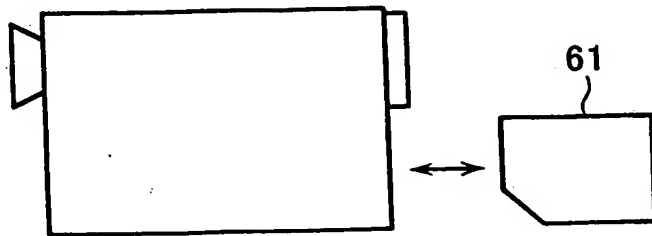


FIG. 19F

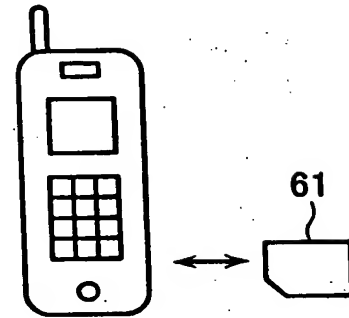


FIG. 19B

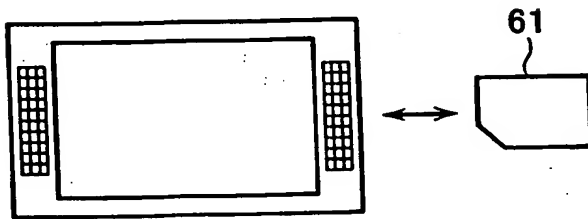


FIG. 19G

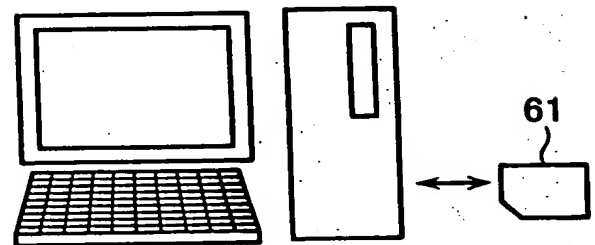


FIG. 19C

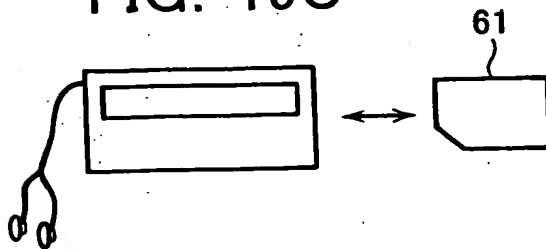


FIG. 19H

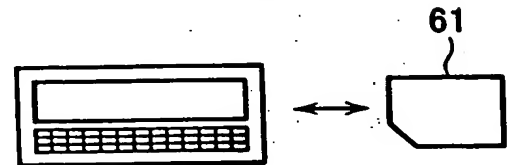


FIG. 19D

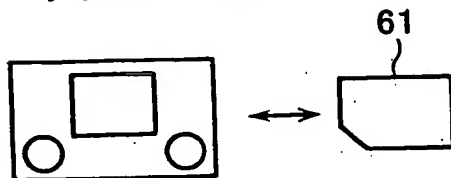


FIG. 19I

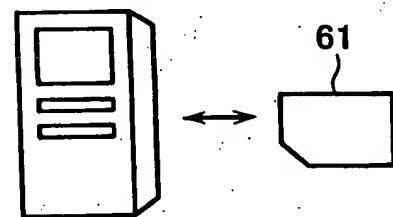


FIG. 19E

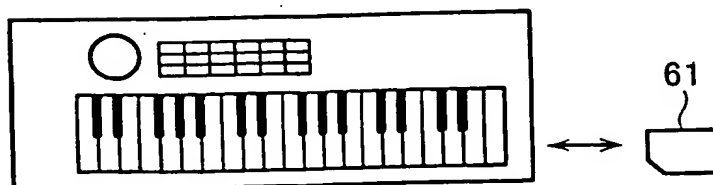


FIG. 19J

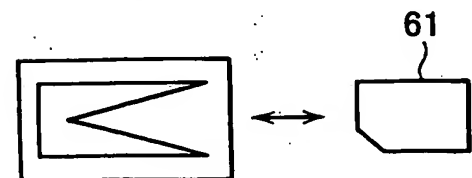




FIG. 20

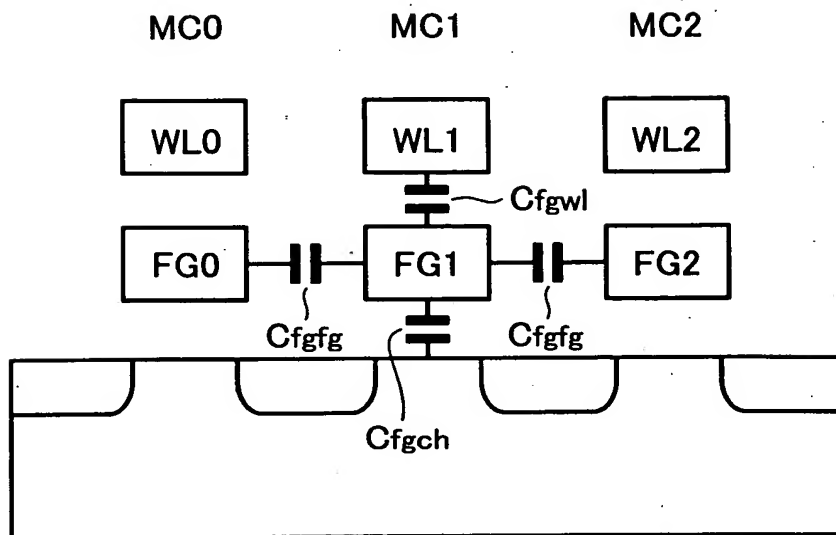


FIG. 21

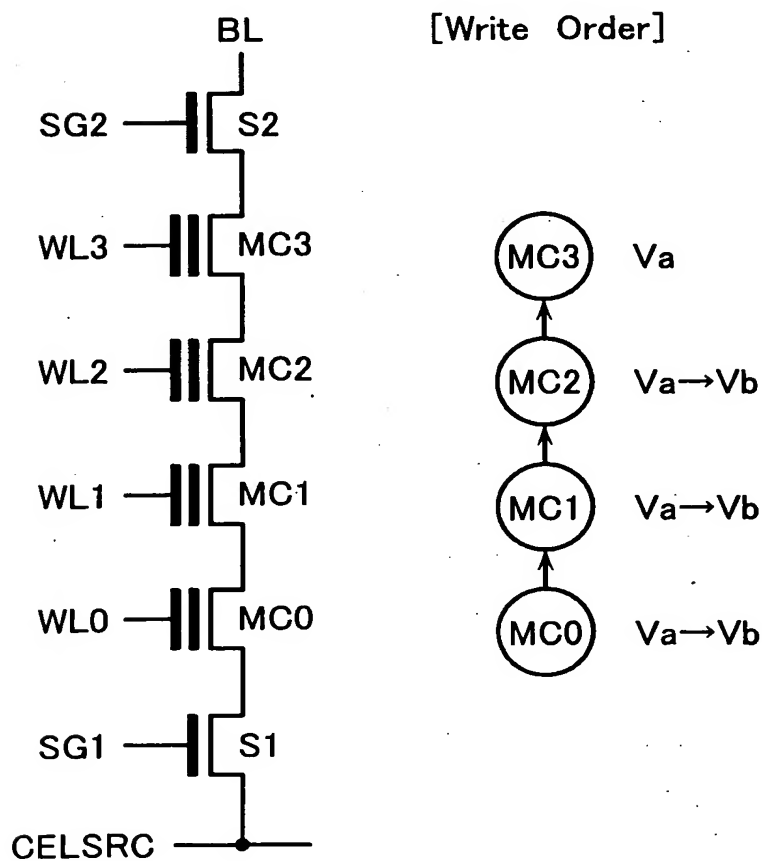




FIG. 22

